## REMARKS

### Claim Rejections – 35 USC § 103

Claims 1, 3-8, and 10-15 are rejected under 35 USC 103(a) as being unpatentable over combinations of U.S. Patent Application Publication No. 2002/0063671 to *Knapp* ("*Knapp*"), U.S. Patent No. 6,236,388 to *Iida et al.* ("*Iida*"), and Japanese Patent No. JP 2000-310767 to *Park et al.* ("*Park*"). Applicants respectfully traverse, noting that no reference discloses every element of the claims as amended. More specifically, no reference discloses sequential and simultaneous scanning of first and third gate lines, after which second gate lines are sequentially scanned. As noted by Examiner, *Knapp* does not disclose the simultaneous scanning of first and third gate lines (Office Action, p. 3). Accordingly, *Knapp* cannot disclose simultaneous and sequential scanning of first and third gate lines, followed by sequential scanning of second gate lines.

*Iida* does not cure the deficiency of *Knapp*. *Iida* at most discloses simultaneous scanning of gate lines, not sequential scanning (e.g., Office Action, p. 3). Moreover, *Iida*'s simultaneous scanning is not followed by sequential scanning of any other area.

*Park* also does not cure the deficiencies of either *Knapp* or *Iida*. *Park* also does not disclose sequential and simultaneous scanning of gate lines, followed by sequential scanning of other gate lines, and thus at least suffers from the same deficiencies as *Iida*.

Thus, none of the above references discloses sequential and simultaneous scanning of first and third gate lines, after which second gate lines are sequentially scanned. Additionally, it follows that none of these references can disclose the sequential scanning of these second gate lines while same data voltages are provided on respective data lines. Applicants' claim 1 as amended is thus patentable over the combination of *Knapp*, *Iida*, and *Park* for at least the reason it recites "wherein the first gate lines are sequentially scanned while the third gate lines are sequentially scanned, after which the second gate lines are sequentially scanned," as well as the additional reason that it recites "wherein same data voltages are provided on the data lines of each pair while the respective second gate lines are scanned." Similarly, Applicants' claim 12 is patentable over these references for at least the reasons that it recites "sequentially applying scanning signals to the first gate lines while the third gate lines are sequentially scanned," "after the applying data voltages for each first pixel and each third pixel, sequentially applying scanning signals to the

second gate lines," and "applying same data voltages for each second pixel to both the respective first and second data lines." The remaining pending claims each depend from one of claim 1 and claim 12, and are thus also patentable for at least these same reasons.

## CONCLUSION

For the reasons stated above, Claims 1, 3-8, and 10-15 are now in condition for allowance. The Directory is hereby authorized to charge any deficiency in fees, or credit any overpayment, to Deposit Account No. 50-2257. Please telephone the undersigned attorney at (408) 392-9250 if there are any questions.

Respectfully submitted,

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